PVP 12

Code: EC7T5A

IV B.Tech - I Semester – Regular Examinations November 2015

ADVANCED VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Answer any **FIVE** questions. All questions carry equal marks

1. a) Find out the noise margin of a CMOS inverter and explain, How the noise margin is affected by voltage scaling? 7 M

   b) What is the lower limit of supply voltage of a CMOS inverter? What happens if the supply voltage equals to inverter threshold voltage? What happens if the supply voltage is further reduced? 7 M

2. Realize the $Z = \overline{(X1 + X2 + X3)(Y1 + Y2)}$ using ECL Circuits. 14 M

3. Realize 8 input complex logic equation
   Z = AB + (C + D) (C + D) + GH using conventional CMOS Logic and Domino CMOS Logic. 14 M

4. Draw and explain the operation of Manchester carry chain adder. 14 M

5. Determine the booth encoded digits E_K for the following words 14 M

a) 10110011

b) 01101101

c) 01010010

6. a) Explain the operation of 1-transistor DRAM cell. 7 M

b) Draw the Block diagram of Random access memory organization and explain its operation. 7 M

7. Write Short notes on 14 M

a) Circuit Synthesis

b) Logic Synthesis

c) Architecture Synthesis

8. What are the components of State Machine? Derive state Machine for 2 bit multiplier. 14 M